Claims

What is claimed is:

1. A system for in-situ surface treatment in fashioning a memory cell comprising:

a gas distribution system that selectively provides a fluorine (F) based gas into a processing chamber; and

an excitation system that electrically excites the fluorine based gas to establish a plasma in the chamber which interacts with the surface to transform the surface from a conductive material into a passive layer that includes a conductivity facilitating compound having conductivity facilitating properties.

2. The system of claim 1 wherein the fluorine based gas includes at least one of CF_4 and SF_6.

3. The system of claim 1 wherein the passive layer includes at least one of copper sulfide (Cu_2S, CuS), copper oxide (CuO, Cu_2O), manganese oxide (MnO_2), titanium dioxide (TiO_2), indium oxide (I_3O_4), silver sulfide (Ag_2S, AgS) and iron oxide (Fe_3O_4).

4. The system of claim 1 wherein the surface is part of an upper portion of a deposition of conductive material placed within and exposed to the plasma by a trench formed within one or more layers of dielectric material spread across a wafer whereon the memory cell fashioning occurs.

5. The system of claim 1 wherein the passive layer has at least one of a thickness range of about 2 Å to about 0.1 μm, about 10 Å to about 0.01 μm and about 50 Å to about 0.005 μm.

6. The system of claim 1 wherein the passive layer has a refractive index from about 2.0 to 2.21.

7. The system of claim 1 wherein the passive layer has a resistivity of about 5.7 x 10^{-2} Ohm/cm.

8. The system of claim 1 wherein the passive layer is transparent with a transmittance of about 60% between 600 and 700 nm.

9. The system of claim 4 wherein a stack formed on a substrate of the wafer comprises the memory cell and includes an organic layer formed over the passive layer and a conductive layer formed over the organic layer, the organic and conductive layers formed within the trench.

10. The system of claim 9 wherein the conductive material under the passive layer serves as a bottom electrode and the conductive layer overlying the organic layer serves as a top electrode.

11. The system of claim 9, the conductive material and the conductive layer including at least one of copper, aluminum, chromium, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, alloys thereof, indium-tin oxide, polysilicon, doped amorphous silicon, metal silicides, Hastelloy®, Kovar®, Invar, Monel®, Inconel®, brass, stainless steel and magnesium-silver alloy.

12. The system of claim 9, the conductive material and the conductive layer having at least one of thickness ranges of about 0.01 μm to about 10 μm, about 0.05 μm to about 5 μm, and about 0.1 μm to about 1 μm.

13. The system of claim 9, the organic layer including at least one of polyacetylene (cis or trans), polyphenylacetylene (cis or trans), polydiphenylacetylene, polyaniline, poly(p-phenylene vinylene), polythiophene, polyporphyrins, porphyrinic macrocycles, thiol derivatized polyporphyrins, polymetallocenes, polyferrocenes, polyphthalocyanines, polyvinylenes and polystiroles.

14. The system of claim 9, the organic layer having at least one of thickness ranges of about 0.001 μm to about 5 μm, about 0.01 μm to about 2.5 μm and about 0.05 μm to about 1 μm.

15. The system of claim 9, the dielectric material including at least one of silicon oxide (SiO), silicon dioxide (SiO_2), silicon nitride (Si_3N_4), (SiN), silicon oxynitride (SiO_xN_y), fluorinated silicon oxide (SiO_xF_y), polysilicon, amorphous silicon, tetraethyorthosilicate (TEOS), phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG).

16. The system of claim 9 wherein a barrier layer at least partially surrounds the conductive material so as to mitigate diffusion of the conductive material into the dielectric material and/or substrate.

17. The system of claim 1 further comprising:

a measurement system that monitors the passive layer being formed;

a control system operatively coupled to the measurement system, gas distribution system and excitation system, the control system obtaining readings taken by the measurement and selectively adjusting at least one of the gas distribution system and excitation system in response thereto to facilitate at least one of forming the passive layer to a desired thickness, forming the passive layer at a desired rate, forming the passive layer to a desired composition and forming the passive layer at a desired location.

18. The system of claim 17 further comprising:

a temperature system that regulates the temperature within the chamber; and

a pressure system that regulates the pressure within the chamber, the control system operatively coupled to the temperature and pressure systems and selectively adjusting at least one thereof in response to readings taken by the measurement system.

19. The system of claim 18 wherein the measurement system is implemented utilizing at least one of optical interference, scatterometry, IR spectroscopy,

ellipsometry, scanning electron microscopy, synchrotron and x-ray diffraction based techniques.

20. The system of claim 1 wherein the excitation system includes a voltage source.

21. A method of treating a surface in situ in fashioning a memory cell on a wafer comprising:

selectively providing a fluorine (F) based gas into a processing chamber;

exciting the fluorine based gas to generate a plasma; and

converting, *via* interaction with the plasma, the surface from a conductive material into a passive layer that includes a conductivity facilitating compound having conductivity facilitating properties.

22. The method of claim 21 further comprising:

measuring at least on of the thickness, rate of formation, composition and location of the passive layer being developed; and

selectively controlling in response to the measurements at least one of pressure within the chamber, temperature within the chamber, concentration of gases within the chamber, rate of flow of gases into the chamber, volume of gases distributed into the chamber and excitation provided within the chamber.

23. The method of claim 22 wherein the measurements are taken *via* at least one of optical interference, scatterometry, IR spectroscopy, ellipsometry, scanning electron microscopy, synchrotron and x-ray diffraction based techniques.

24. The method of claim 22 further comprising:

mapping the wafer into one or more grids; and

obtaining measurements at the grid mapped locations.

25. The method of claim 21 wherein the fluorine based gas includes at least one of CF_4 and SF_6.

26. The method of claim 21 wherein the passive layer includes at least one of copper sulfide (Cu_2S, CuS), copper oxide (CuO, Cu_2O), manganese oxide (MnO_2), titanium dioxide (TiO_2), indium oxide (I_3O_4), silver sulfide (Ag_2S, AgS) and iron oxide (Fe_3O_4), the method further comprising:

forming the passive layer to have at least one of a refractive index from about 2.0 to 2.21, a resistivity of about 5.7×10^{-2} Ohm/cm, a transparency with a transmittance of about 60% between 600 and 700 nm and a thickness between about 200 to 600 nm.

27. The method of claim 21 wherein the surface is part of an upper portion of a deposition of conductive material placed within and exposed to the plasma by a trench formed within one or more layers of dielectric material spread across the wafer.

28. The method of claim 27 wherein a stack formed on a substrate of the wafer comprises the memory cell and includes an organic layer formed over the passive layer and a conductive layer formed over the organic layer, the organic and conductive layers formed within the trench.

29. The method of claim 28 wherein the conductive material under the passive layer serves as a bottom electrode and the conductive layer overlying the organic layer serves as a top electrode.

30. The method of claim 28, the conductive material and the conductive layer including at least one of copper, aluminum, chromium, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, alloys thereof, indium-tin oxide, polysilicon, doped amorphous silicon, metal silicides, Hastelloy®, Kovar®, Invar, Monel®, Inconel®, brass, stainless steel and magnesium-silver alloy.

31. The method of claim 28, the organic layer including at least one of polyacetylene (cis or trans), polyphenylacetylene (cis or trans), polydiphenylacetylene, polyaniline, poly(p-phenylene vinylene), polythiophene, polyporphyrins, porphyrinic macrocycles, thiol derivatized polyporphyrins,

polymetallocenes, polyferrocenes, polyphthalocyanines, polyvinylenes and polystiroles.

32. The method of claim 28, the dielectric material including at least one of silicon oxide (SiO), silicon dioxide (SiO_2), silicon nitride (Si_3N_4), (SiN), silicon oxynitride (SiO_xN_y), fluorinated silicon oxide (SiO_xF_y), polysilicon, amorphous silicon, tetraethyorthosilicate (TEOS), phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG).

33. The method of claim 28 further comprising:

forming a barrier layer that at least partially surrounds the conductive material so as to mitigate diffusion of the conductive material into the dielectric material and/or substrate.

34. A memory cell comprising:

a deposit of conductive material that serves as a bottom electrode, the bottom electrode formed on a substrate on a wafer and in a trench formed within a dielectric material spread across the wafer;

a passive layer having conductivity facilitating properties, the passive layer formed out of an upper portion of the bottom electrode *via* a plasma which interacts with the conductive material to convert the upper portion of the bottom electrode so as to include, at least, a conductivity facilitating compound, the plasma being generated from a fluorine (F) based gas and having access to the upper portion of the bottom electrode by way of the trench;

an organic layer formed over the passive layer; and

a layer of conductive material formed over the organic layer to serve as a top electrode.

35. The memory cell of claim 34 further comprising:

a barrier layer that at least partially surrounds the bottom electrode so as to mitigate diffusion of the conductive material into the dielectric material and/or substrate.

36. The memory cell of claim 34 wherein the bottom and top electrodes include at least one of copper, aluminum, chromium, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, alloys thereof, indium-tin oxide, polysilicon, doped amorphous silicon, metal silicides, Hastelloy®, Kovar®, Invar, Monel®, Inconel®, brass, stainless steel and magnesium-silver alloy.

37. The memory cell of claim 34 wherein the organic layer includes at least one of polyacetylene (cis or trans), polyphenylacetylene (cis or trans), polydiphenylacetylene, polyaniline, poly(p-phenylene vinylene), polythiophene, polyporphyrins, porphyrinic macrocycles, thiol derivatized polyporphyrins, polymetallocenes, polyferrocenes, polyphthalocyanines, polyvinylenes and polystiroles.